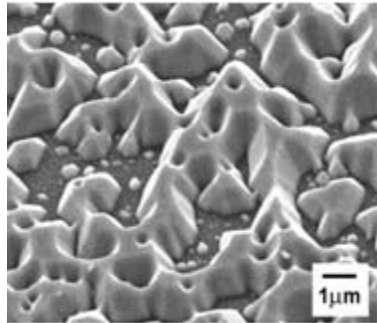
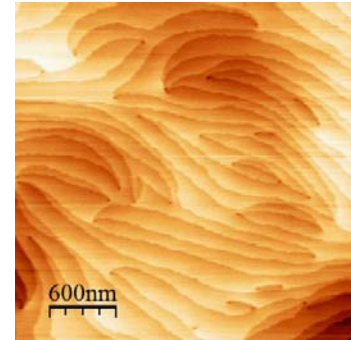




# Improving Epitaxial Growth for LEDs



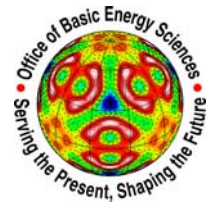
**Daniel D. Koleske**



**Sandia National Laboratories**



This work supported by the Energy Efficiency and Renewable Energy (EERE) and the Office of Basic Research at the U.S. Department of Energy.





# Two New Research Facilities and National Lab Center for SSL R&D



**DOE Sec. Bodman announced the National Center for SSL R&D**



**Sandia has been designated the lead lab of the National Center**

**CINT Core Facility in Albuquerque**



**CINT Gateway to Los Alamos**



**Microfab**



**Microlab**

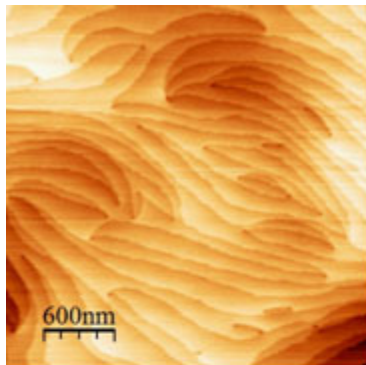


**Microsystems and Engineering Sciences Applications (MESA)**

# Major Technological Issues Associated with Group III-N Epitaxy

## 1) Lack of a GaN substrate

Grow on sapphire or SiC



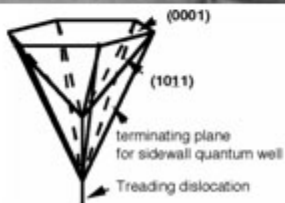
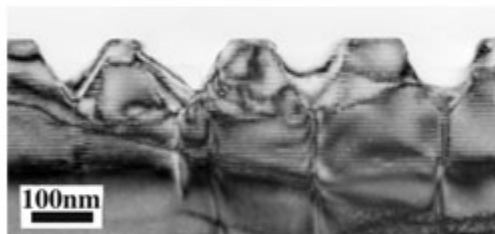
Results large numbers of dislocations.

Dislocations trigger



## 2) Defect formation in the InGaN layers

V-defects form at dislocation cores. Also have point and impurity defects.

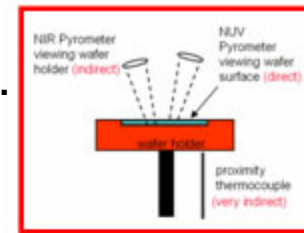


Dislocation

Exact influence of V-defect on LED performance is still under investigation.

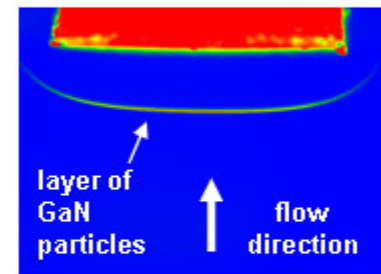
## 3) Temperature measurement and InGaN stability

- Visible and IR pyrometers do not measure substrate growth temperature.
- Indium incorporation depends strongly on growth temperature.



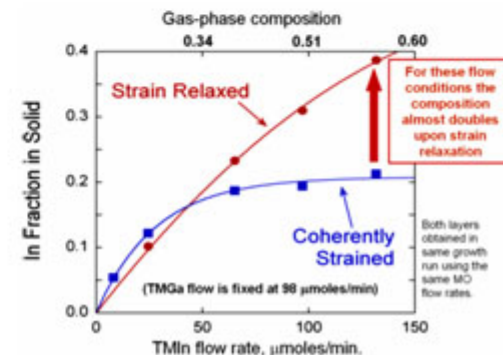
## 4) Group III-N MOCVD growth conditions.

- Gas phase parasitic reactions.
- InGaN growth in only  $N_2$ , no  $H_2$ .
- Metallic indium on surface.



## 5) Compressive strain of InGaN on GaN

- Strain increases as the indium content and film thickness increase.
- Relieving strain creates undesired defects.
- Indium content may be limited to  $\leq 20\%$ .

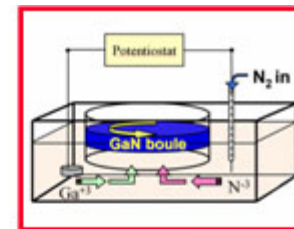




# Group III-N Epitaxy Research Programs at Sandia

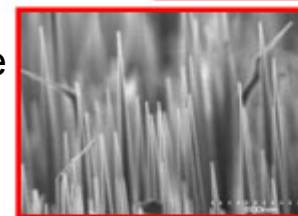
## 1). Lack of a GaN substrate.

- ✓ “Development of Bulk Gallium Nitride Growth Technique for Low Defect Density Large Area Native Substrates” – PI: *Karen Waldrip* – NETL – 2nd year.
- ✓ “Nanowire Templated Lateral Epitaxial Growth of Low Dislocation Density GaN” PI: *George Wang* – NETL – 2<sup>nd</sup> year (18 months).
- ✓ “Nanostructural Engineering of Nitride Nucleation Layers for GaN Substrate Dislocation Reduction” – PI: *Dan Koleske* – 2<sup>nd</sup> year (18 months).



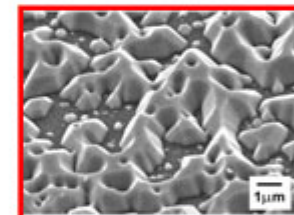
## 2). Defect formation in the InGaN layers.

“Luminescence, Structure, and Growth of Wide-Bandgap Semiconductors” PI: *Steve Lee* – BES – ongoing.



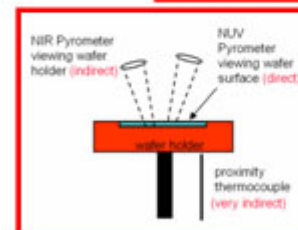
## 3). Temperature measurement and InGaN stability.

- ✓ “Improved InGaN Epitaxy Yield by Precise Temperature Measurement” PI: *Randy Creighton* – NETL – completed.



## 4). Group III-N MOCVD growth conditions.

“Improved InGaN Epitaxial Quality by Optimizing Growth Chemistry” PI: *Randy Creighton* – NETL – “new”.



## 5). Compressive strain of InGaN on GaN.

- ✓ “Innovative Strain Engineered InGaN Materials of High Efficiency Green Light Emission” – PI: *Mike Coltrin* - NETL – 2<sup>nd</sup> year



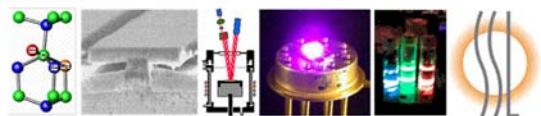
# Sandia's Grand Challenge LDRD on Solid-State Lighting began in 2000

## Goals of the Grand Challenge:

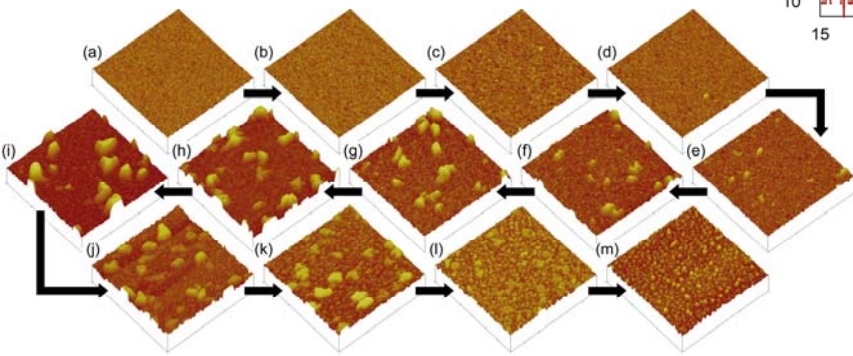
1. Help establish the fundamental science and technology base for SSL.
2. Develop the technology infrastructure for Group III-nitride material sciences for synergistic national security needs.

At the end of FY04, this project had invested ~\$8M internal funds on SSL  
Built on Sandia's investment of **several \$100 M in compound semiconductor technology** over more than 20 years.

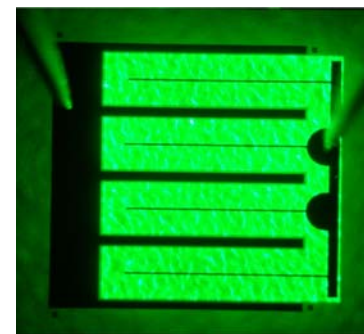
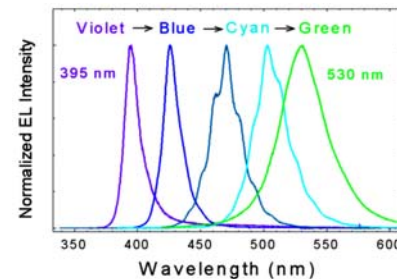
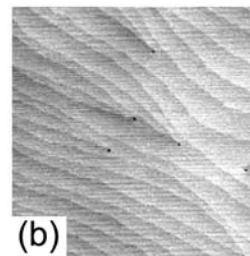
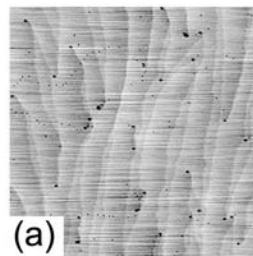
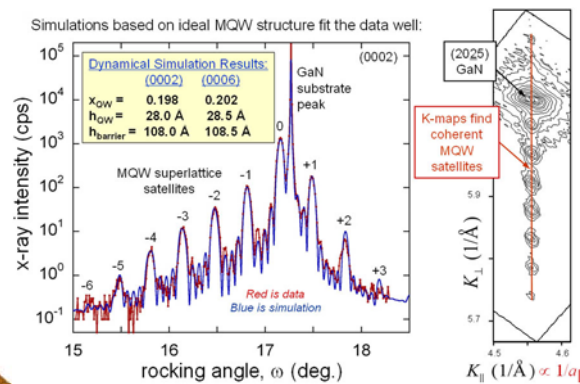
### Final Report on Grand Challenge LDRD Project:



A Revolution in Lighting –  
Building the Science and Technology Base  
for Ultra-Efficient Solid-State Lighting



Simulations based on ideal MQW structure fit the data well:





## Building Technologies Program

### Solid-State Lighting

[Why Invest in SSL?](#)

[SSL Portfolio Plan](#)

[Research Highlights](#)

[Project Portfolio](#)

[Funding Opportunities](#)

[Publications](#)

[FAQs on Market-Available LEDs](#)

[Home](#)

#### Cantilever Epitaxy Process Wins R&D 100 Award

Sandia National Laboratories received an R&D 100 Award from *R&D Magazine* for development of a new process for growing gallium nitride on an etched sapphire substrate. The process, called cantilever epitaxy, promises to make brighter and more efficient green, blue, and white LEDs.

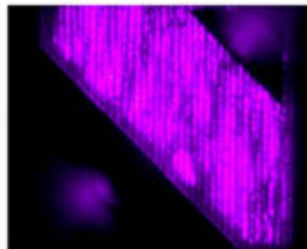
The cantilever epitaxy process eliminates many of the problems that limit the performance of LEDs grown on sapphire/gallium nitride substrates. In the past few years, LEDs have been grown with various combinations of gallium nitride alloys on sapphire substrates. In the process, regions of imperfections – called dislocations – are formed, which limit LED brightness and performance. The cantilever epitaxy process reduces the number of dislocations, offering the potential for longer-lived and better performing LEDs.

#### Reducing Dislocation Density Through GaN Cantilever Growth

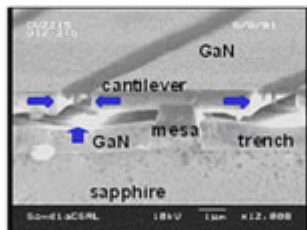
Sandia's cantilever epitaxy growth process begins with etching trenches into the sapphire substrate, leaving stripes of mesas in the surface. Vertical growth of the GaN overlayer is then initiated on the mesas. After some vertical growth, the conditions of the growth reactor are adjusted to produce lateral growth over the trenches. This lateral cantilever material – suspended by the mesas – does not contain dislocations because it is not in contact with the substrate. After adjacent cantilevers are grown together, the material is grown vertically to produce the desired thickness. In the end, dislocations produced by contact with the substrates are confined to the mesa areas, and the cantilever regions over the trenches have very low dislocation densities.

The cantilever epitaxy research conducted at Sandia was supported in part by an internal Laboratory Directed Research and Development (LDRD) Grand Challenge, and in part by a cooperative agreement from DOE (Office of Energy Efficiency and Renewable Energy, Building Technologies Program) for a collaborative project with LumiLeds Lighting.

For more information on cantilever epitaxy, see the [Sandia/LumiLeds Research Highlights](#) and the [Sandia National Laboratories News Release](#).

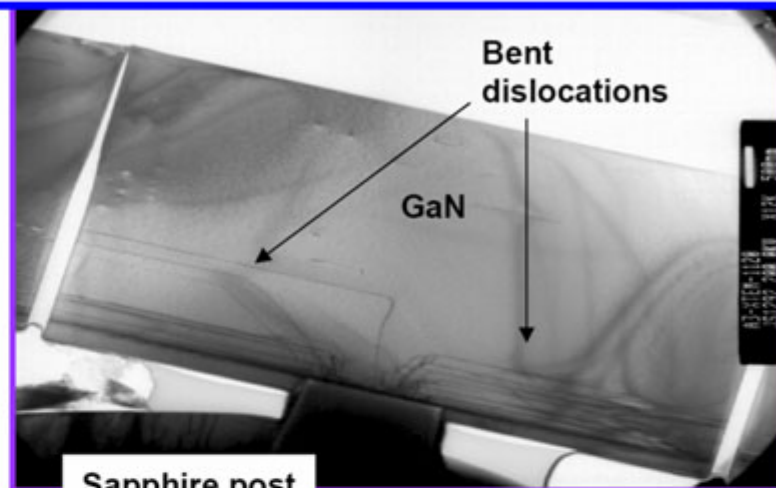


An electroluminescence image of an LED fabricated using the cantilever epitaxy process shows uniform LED intensity over multiple regions.



A cross-sectional microscope image shows GaN cantilevers growing toward each other with GaN growing upward in the trenches.

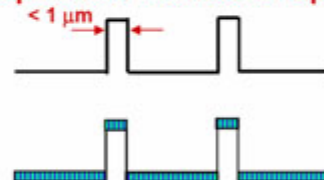
# R&D 100 Research Award in 2004



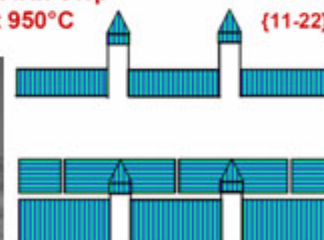
Sapphire post

**Goal: Develop low-dislocation density GaN substrate**

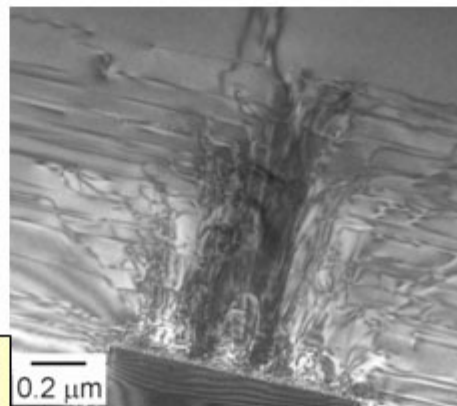
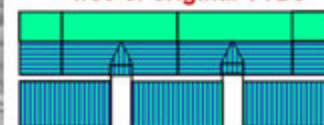
**Sandia patented "Cantilever Epitaxy"**



**Facet Growth Step**  
0.5  $\mu\text{m}$  at 950°C



**< 1/50 of original VTDs**



**R&D 100 Award, 2004**

SNL: Follstaedt et al., APL, 2002

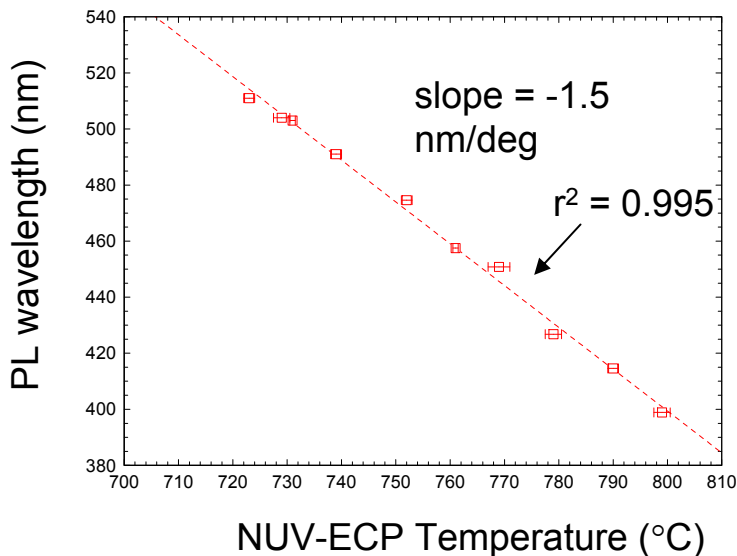
**CE later used in the "LED Substrates and New Materials" NETL funded program with LumiLeds.**



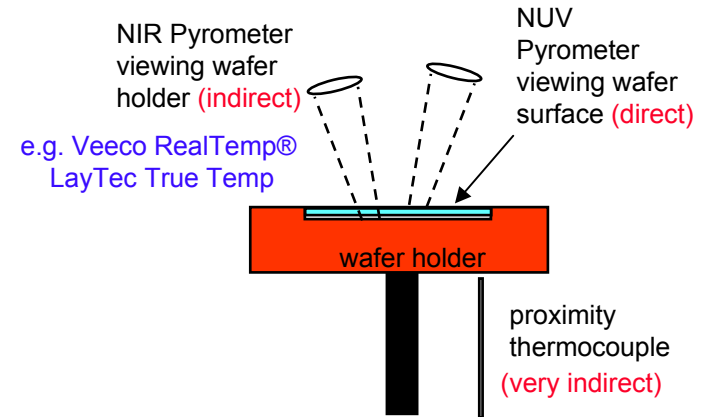
# “Improved InGaN Epitaxy Yield by Precise Temperature Measurement” – Randy Creighton

**Goal: Develop a pyrometer that measures the “true” surface temperature.**

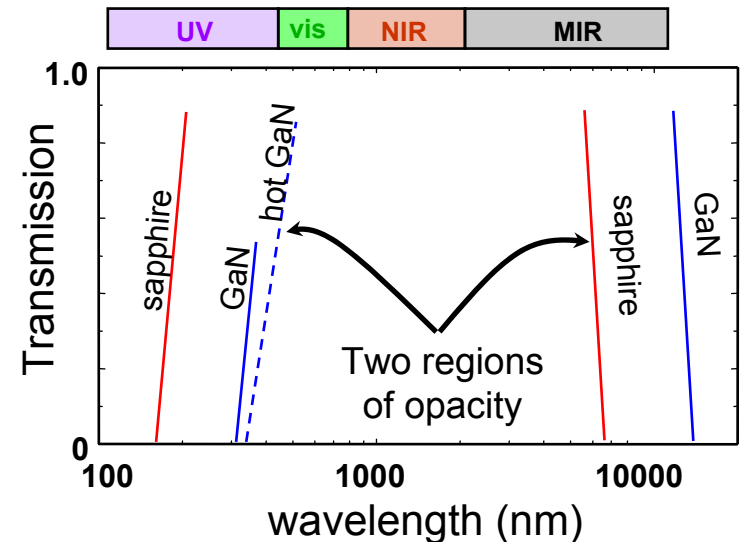
**Background: There is a strong temperature dependence on indium incorporation**



**Various methods of temperature measurement are used with different levels of success.**



**Randy’s idea focus on 400 nm and 7 μm wavelengths**



## Project Team:

PI - Randy Creighton

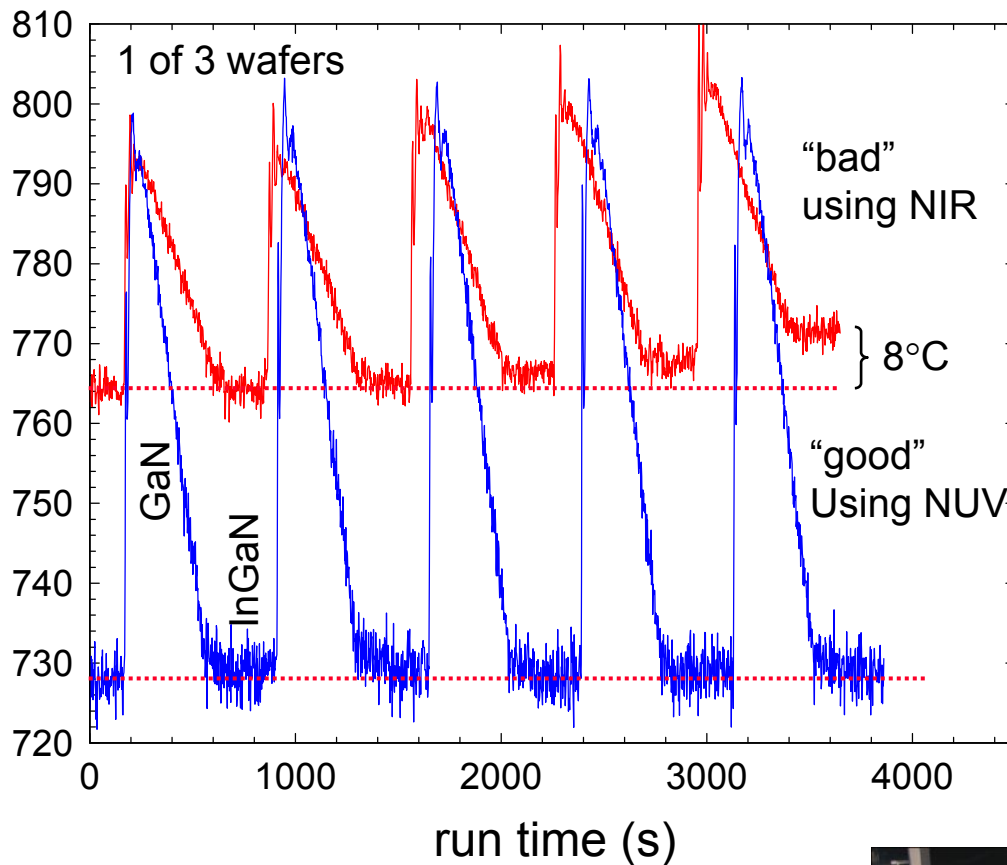
Growth - D.D. Koleske, G. Thaler, and M.J. Russell

Pyrometry expertise – Bill Breiland, PL - Art Fischer

Early contributions – C.C. Mitchell and K.E. Waldrip

# “Improved InGaN Epitaxy Yield by Precise Temperature Measurement” – Randy Creighton

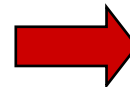
NUV Temperature



First true NUV pyrometer developed at Sandia by Randy Creighton, JCG 287, 572 (2006).

Last year Laytec developed a commercial UV pyrometer based on research at Sandia.

NETL funded research at Sandia



Commercial product

## FEATURE

compoundsemiconductor.net

May 3, 2007

## UV tool maps nitride temperatures

LayTec is targeting GaN chip developers with an in situ pyrometer that can measure wafer temperatures with a precision of  $\pm 0.1$  °C. Richard Stevenson investigates.

Profitable chip making demands low development costs and high production yields. To cut expense, growth recipes should be established using minimal runs, because this optimization process can consume a large proportion of the development budget. To do this, process engineers must know as much as possible about the reactor's local environment, including wafer temperature - a primary driver of epilayer growth rates and compositions.

Pyrometry is the standard method for measuring the wafer's temperatures within a reactor. The technique involves measuring the intensity of thermal radiation emitted by the wafers over a narrow wavelength band using a photodetector, and then correlating this intensity to a temperature. The temperature of wafers based on InP and GaAs material systems can be measured with a pyrometer operating at 950nm. However, this spectral region is useless for nitrides, because they do not produce any radiation at this wavelength.



Pyro 400

To address this deficiency, pyrometers that operate at 400 nm have been built for nitride growth. The first of these was constructed by JoRandall Creighton and co-workers from Sandia National Laboratories, NM, and last year in situ monitoring specialist LayTec introduced a commercial version of this tool, the Pyro 400, at the MRS fall meeting in Boston, MA. This instrument is primarily designed for Aixtron multi-wafer reactors, but could be adapted for Thomas Swan tools.



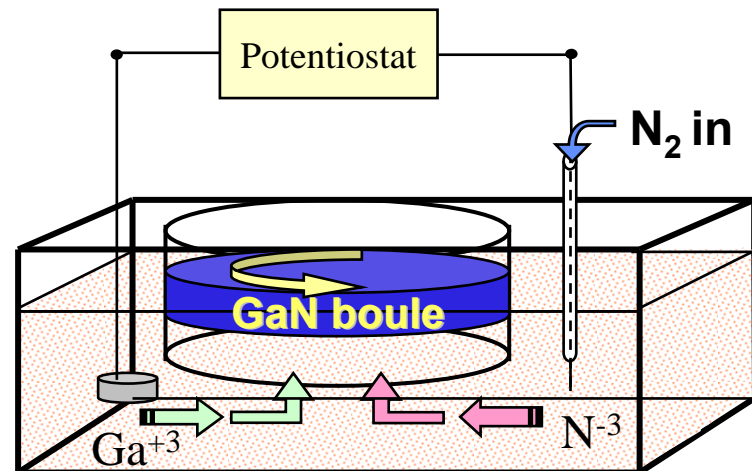


# “Development of Bulk Gallium Nitride Growth Technique for Low Defect Density Large Area Native Substrates” – Karen Waldrip

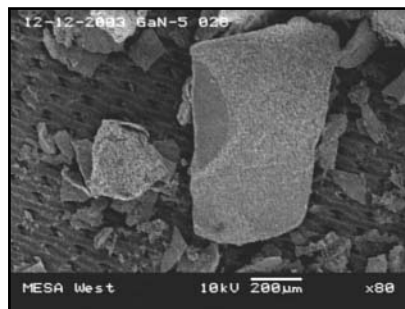


## Goal: Obtain bulk mm-sized GaN crystals

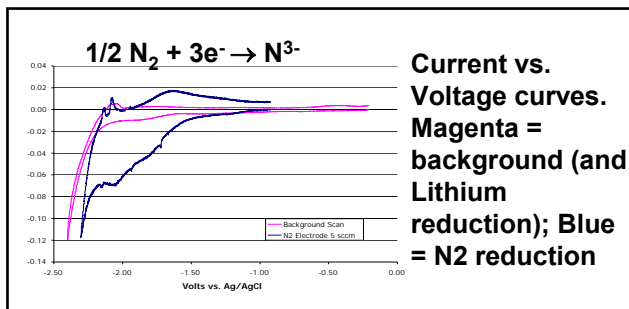
- Nitrogen gas reaction kinetics slow, thermodynamics cumbersome.
- Goto and Ito (Kyoto University) have demonstrated continuous and nearly quantitative electrochemical reduction of nitrogen gas in a molten chloride salt.
- Gallium oxidation is straightforward.
- $\text{Ga}^{+3}$  and  $\text{N}^{-3}$  are very soluble in molten salt.
- Our novel approach: crack precursors electrochemically and precipitate crystal from solution!
- Inexpensive, large-area boules may be possible.



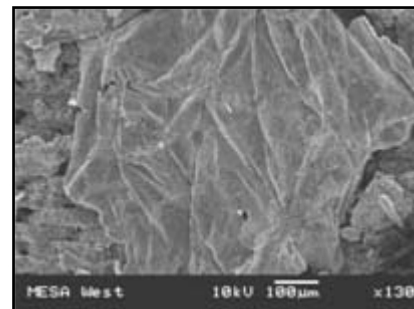
\*All discrete parts of approach have now been demonstrated in proof-of-concept form with minimal investment in equipment; more sophisticated equipment necessary to combine experimental elements and make further improvements.



0.9x0.6mm grown in 2hrs (vs. state of the art 1cm<sup>2</sup> x 100 µm in 30+ days)

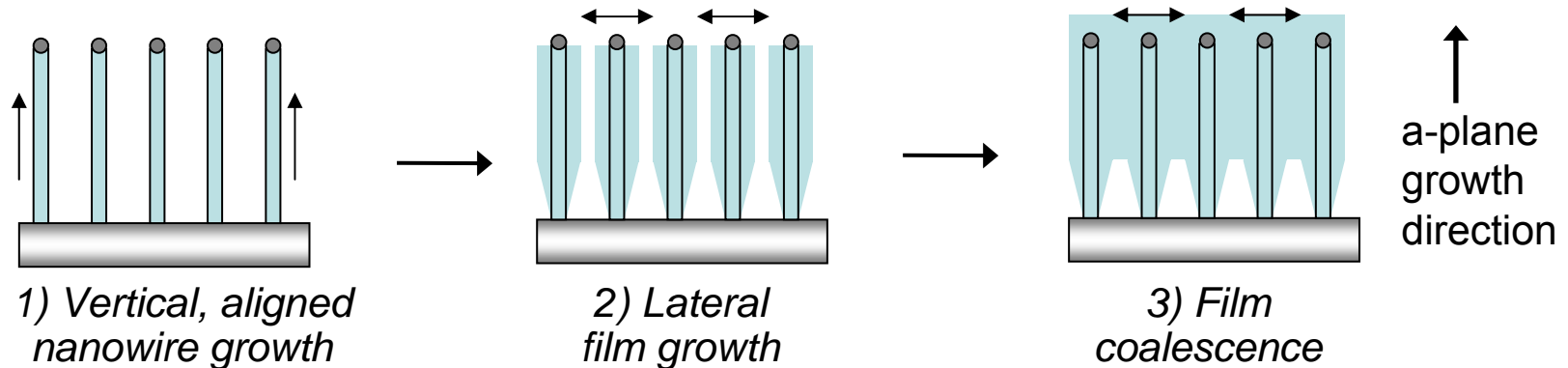


Current vs. Voltage curves. Magenta = background (and Lithium reduction); Blue = N<sub>2</sub> reduction



0.9 x 1.25mm crystal with 120° hexagonal facets

# “Nanowire Templated Lateral Epitaxial Growth of Low Dislocation Density GaN” - George Wang



**Goal:** To develop a novel, low-cost technique employing vertically aligned GaN nanowire arrays for reduced dislocation density GaN.

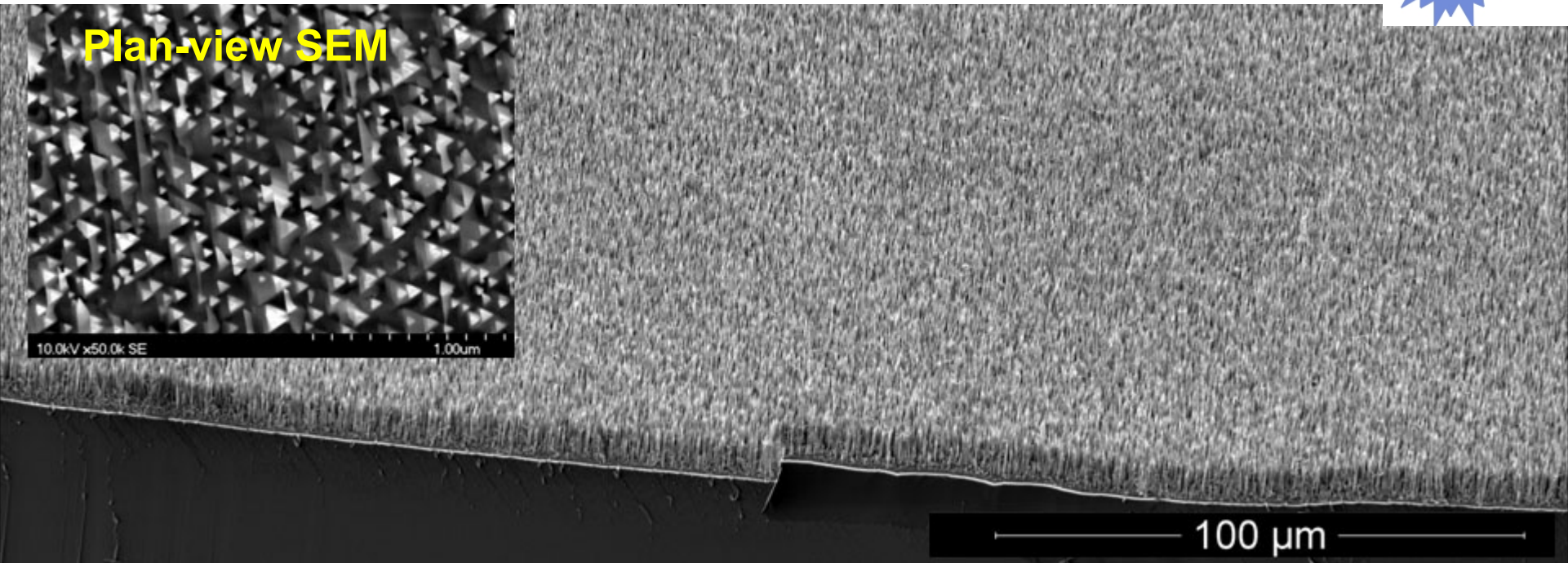
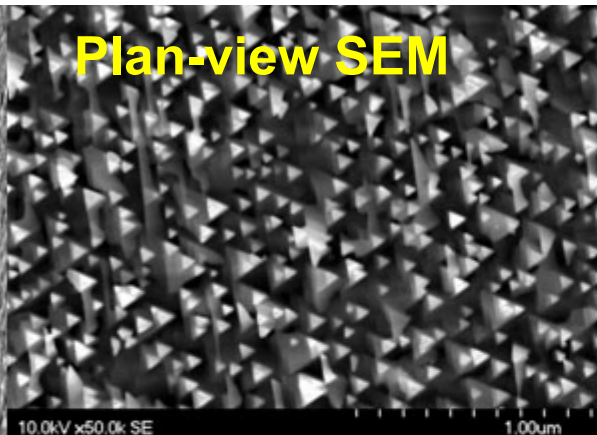
## Advantages of NTLEG approach

- Dislocation-free nanowire arrays serve as growth template
- **Nanowires serve as 3D-compliant nanoscale bridges connecting film and substrate, relieving strain in the film & reducing defects (nanoheteroepitaxy)**
- Low cost
  - Sapphire can be used (potentially even Si)
  - Requires *no patterning or interruption of growth*
  - Cost is comparable to standard GaN growth on sapphire
- **Film takes on nanowire orientation (non-polar orientations available)**

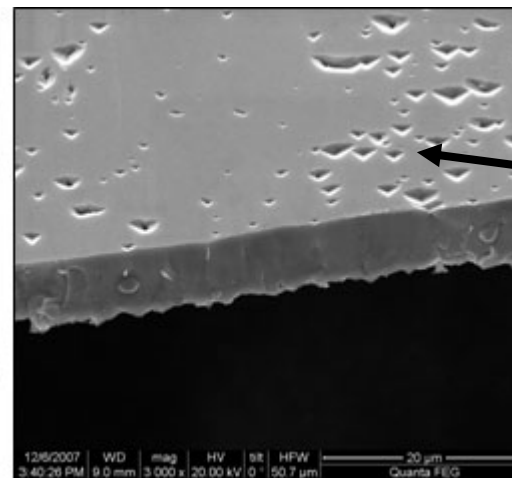
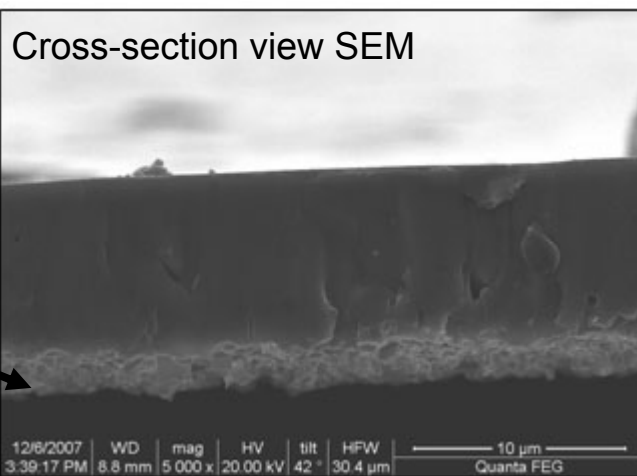
# Dense, uniform, vertically aligned growth of GaN nanowires on sapphire over 2" wafer



Plan-view SEM



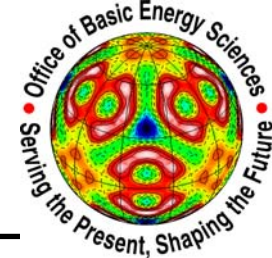
Fully coalesced a-plane NTLEG GaN films demonstrated from nanowire templates



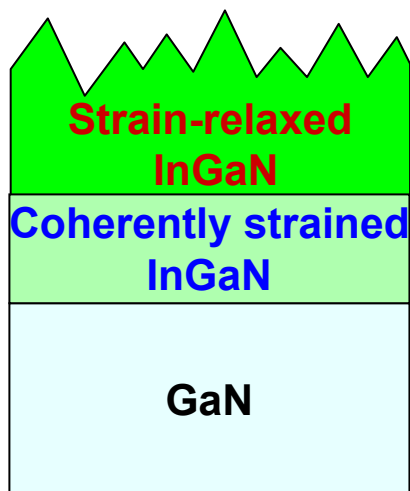
“Free-standing”  
NTLEG GaN film  
(nanowires facilitate  
film removal from  
substrate)



# “Luminescence, Structure, and Growth of Wide-Bandgap Semiconductors” – Steve Lee



~100-nm-thick InGaN  
on GaN at 760 C:

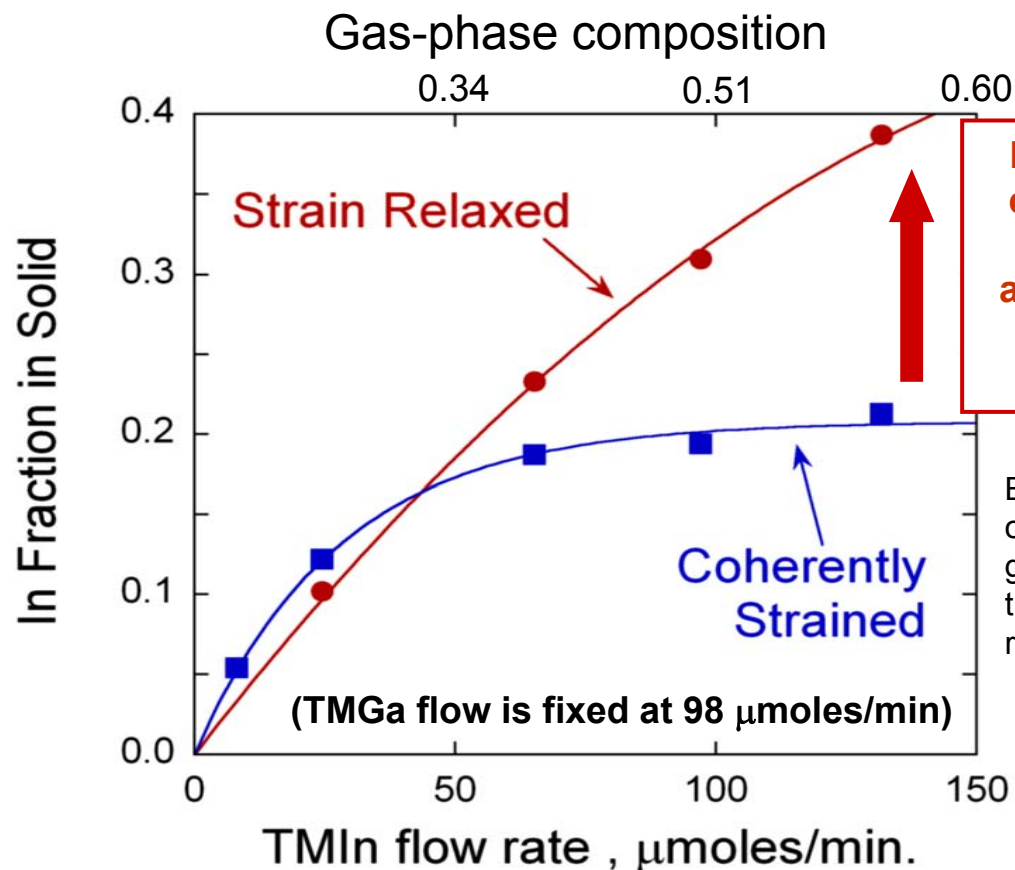


## Related observations:

Z. Liliental-Weber, et al., J. Electron. Mat. **30** ('01) 439.

S. Pereira, et al., APL **80** ('02) 3913.

Shimizu, et al., JJAP **36** ('97) 3381.

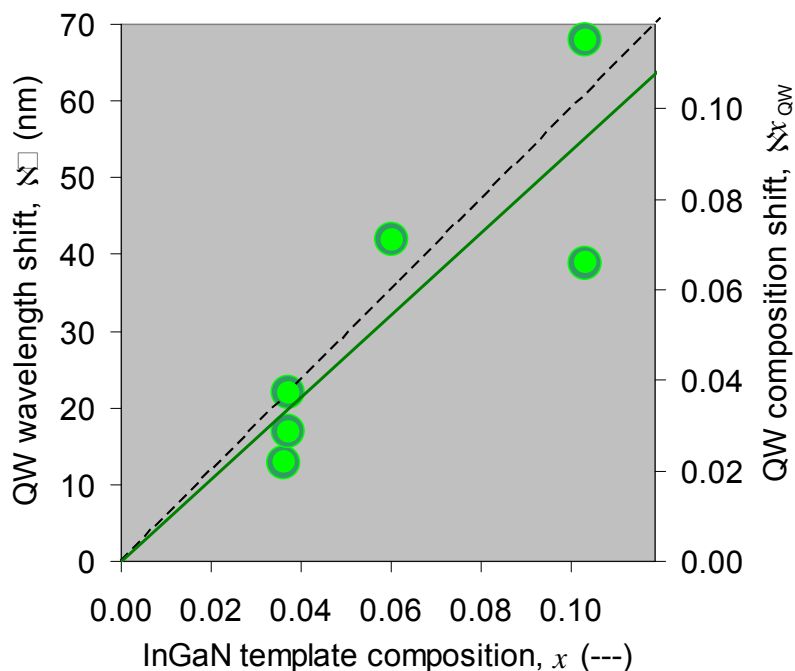


**Need to develop strain relaxed InGaN layers for indium content > 0.2**

# Innovative Strain Engineered InGaN Materials of High Efficiency Green Light Emission – Mike Coltrin



growth run #	GaN template, $\lambda_{\text{QW}}$ (nm)	InGaN template, $\lambda_{\text{QW}}$ (nm)	$\Delta\lambda_{\text{QW}}$ (nm)	InGaN template, $x$ (---)	InGaN QWs, $\Delta x_{\text{QW}}$ (---)
dnz01166	431	444	13	0.036	0.022
dnz01254	---	479	42	0.060	0.071
dnz01299	442	466	22	0.037	0.037
dnz01376	463	531	68	0.103	0.115
dnz01439	429	446	17	0.037	0.029
dnz01439	429	468	39	0.103	0.066



- QW emission shifts to longer wavelength on strain-relaxed InGaN templates
- This implies that In-composition of QWs increases with In-composition of the strain-relaxed InGaN template
- Nominal QW compositions on standard GaN templates were  $x_{\text{QW}} \sim 0.13-0.16$
- Compositions of similarly grown QWs on relaxed  $\text{In}_{0.10}\text{Ga}_{0.90}\text{N}$  approach  $x_{\text{QW}} \sim 0.26$
- Increase in InGaN QW composition is directly proportional to the composition of the relaxed InGaN template

## Conclusions:

- Fundamental premise of the project is confirmed
- QW emission at 531 nm exceeds 1<sup>st</sup> year milestone (505 nm)

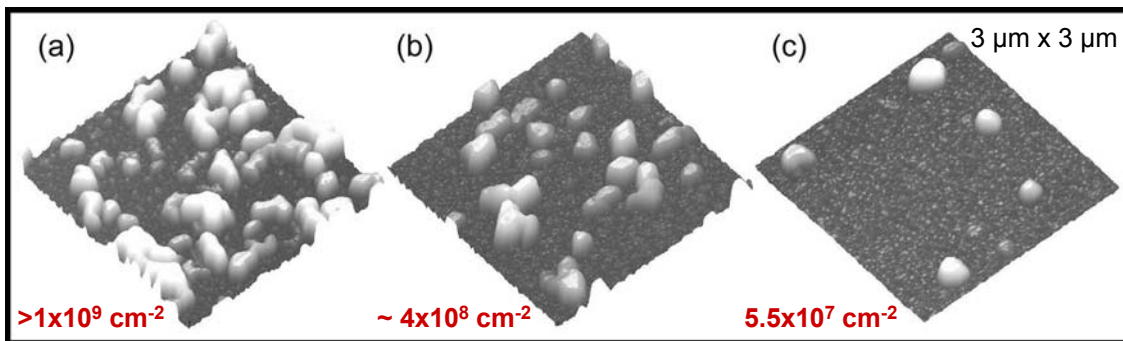
# “Nanostructural Engineering of Nitride Nucleation Layers for GaN Substrate Dislocation Reduction” – Dan Koleske

**Goal: Routinely achieve dislocation densities of  $\sim 1 \times 10^8 \text{ cm}^{-2}$  on sapphire without too much additional growth overhead**

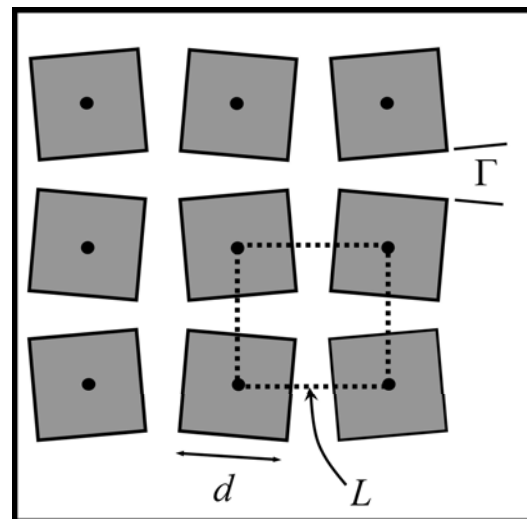
**Approach: Reduce the GaN nucleation site density on sapphire, establish oriented GaN grains, and coalesce films without the formation of additional nuclei.**

If lower dislocation density substrates existed then...

- 1) Improve epitaxial quality – smoother surfaces & interfaces.
- 2) Reduce density of V-defects in green InGaN QWs & LEDs.
- 3) Dislocation mediated degradation should be reduced.



Using a simple geometric model for the dislocation,  $\rho$ , generation vs. the nucleation density,  $n_D$



**Case 1: Dislocations are generated along tilt boundaries.**

$$\rho \approx (2\Gamma/Kb) n_D^{1/2}$$

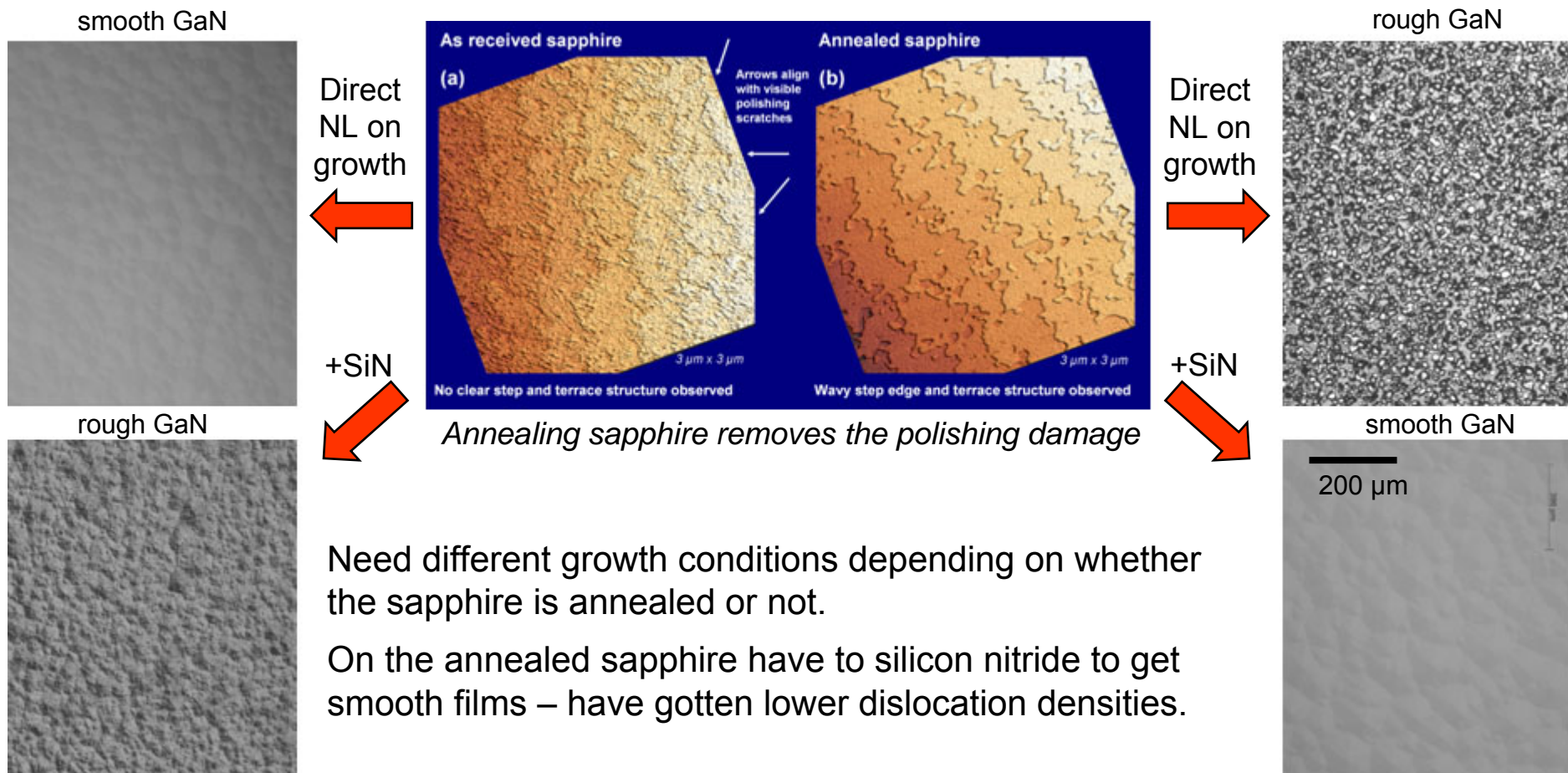
**Case 2: Dislocations are generated within each nuclei.**

$$\rho \approx n_D$$



# “Nanostructural Engineering of Nitride Nucleation Layers for GaN Substrate Dislocation Reduction” – Dan Koleske

Dislocation density measured using XRD – Lee *et al.* APL 86, 241904 (2005).  
Best dislocation density for simple two step (NL + HT) GaN on sapphire is  $4.0 \times 10^8 \text{ cm}^{-2}$



Need different growth conditions depending on whether the sapphire is annealed or not.

On the annealed sapphire have to silicon nitride to get smooth films – have gotten lower dislocation densities.

Using the current process dislocation densities of  $\sim 2.5 \times 10^8 \text{ cm}^{-2}$  were achieved.



## Thanks to:

---

**NETL Program Managers:  
Joel Chaddock • Ryan Egidi •  
Morgan Pattison • Brian Dotson**

### Sandia Colleagues:

S. R. Lee – XRD analysis

M. E. Coltrin – modeling

M. H. Crawford – PL, LED studies

A. J. Fischer – PL, photonics

G. Thaler – MOCVD growth

J. R. Creighton – InGaN chemistry

G. T. Wang – nanowire growth

Q. Li – MOCVD nanowire growth

D. M. Follstaedt – TEM microscopy

N. A. Missert – CL imaging

K. E. Waldrip – GaN bulk growth

J. J. Figiel – MOCVD tech.

M. J. Russell – MOCVD tech.

M. Banas – PL tech.

R. M. Biefeld – manager 1126

D. L. Barton – manager 1123